**CLAIMS:**

1. A voltage monitoring system configured for monitoring a DC voltage of a differential line pair with respect to a threshold voltage, comprising:

a detection circuit comprising a first line and a second line, each line connectable to one of the two lines of the differential line pair, said detection circuit further comprising:

a low pass filter configured and disposed in relation to the first and second lines to pass a DC signal of steady state or low-frequency voltage swing from the differential line pair to the rest of the detection circuit, and to block a pulse signal from a microcontroller set forth herein below from passing between the first and second lines;

a bias circuit portion comprising at least one Zener diode, disposed between the first and second lines and configured to allow current to flow, and accordingly to pass said pulse signal, between the first and second lines when the voltage across the differential line pair is above a selected breakdown voltage of the Zener diode;

a DC isolation portion comprising a pair of capacitors disposed in the first and second lines, said DC isolation portion configured to pass said pulse signal, and to impede other DC signals from the differential line pair from passing from the differential line pair to said microcontroller; and,

said microcontroller, configured to send and detect pulse signals, and to detect when the DC voltage across the line pair is at least one of above and below the threshold value, and to thus enable monitoring of the differential line pair in this respect;

the low pass filter being disposed between the line pair and the other elements of the detection system, the bias circuit portion being disposed between the low pass filter and the DC isolation portion, and the DC isolation portion being disposed between the bias circuit portion and the microcontroller, pulse signals being passed or not passed between the first and second lines depending on whether the DC voltage across the differential line pair is above or below the breakdown voltage of the bias circuit diode being detectable by the microcontroller, and said low pass filter impeding said pulse signals from traveling out onto the differential line pair and said DC isolation portion impeding DC signals from interfering with the microcontroller and isolating the differential line pair from the microcontroller and other elements which are connectable thereto.

2. A system as set forth in claim 1, wherein said system is configured for monitoring a differential line pair of a POTS line.

3. A system as set forth in claim 2, wherein said system is configured to monitor at least one of an on hook and an off hook DC voltage state of said POTS line.

4. A system as set forth in claim 1, wherein the bias circuit portion comprises a plurality of Zener diodes and the system enables monitoring of the differential line pair without knowing its polarity.

5. A system as set forth in claim 3, wherein a breakdown voltage of a Zener diode of the bias circuit portion is selected as a threshold voltage such that voltages across the line pair in an on hook state are above the threshold voltage and voltages across the line pair in an off hook state are below the threshold voltage.

6. A system as set forth in claim 5, wherein the microcontroller is configured to detect a ring condition on the POTS line.

7. A system as set forth in claim 6, wherein said ring condition is detected by counting voltage swings across the threshold voltage over a selected time interval.

8. A system as set forth in claim 7, wherein the system is configured to detect a first ring and then signal an enablement of a read of caller ID information during a time interval between said first ring and a second ring.

9. A system as set forth in claim 8, wherein the system is configured to ignore caller ID signals at other times.

10. A telephone system monitoring system configured to detect at least one of on hook and off hook DC states of a differential POTS line pair, comprising:

a detection circuit configured to isolate the line pair from the rest of the detection circuit by means of capacitors in the line pair; said detection circuit further comprising means for sending pulse signals across the capacitors and means for returning or preventing return

of the pulse signals depending upon whether the DC voltage differential across the line pair is above or below a selected threshold value;

means for indicating whether the voltage across the differential line pair is at least one of above or below the threshold value.

11. A system as set forth in claim 10, further comprising means for detecting a ring condition on the POTS line.

12. A system as set forth in claim 10, further comprising means for indicating initiation and termination of a call based on differentiating an on hook and an off hook DC voltage state corresponding to the DC voltage across the differential line pair being above or below the threshold voltage.

13. A system as set forth in claim 11, further comprising means for identifying a window for capturing caller ID information in a signal carried by the differential line pair.

14. A system as set forth in claim 10, wherein the means for sending pulse signals includes an appropriately programmed microcontroller.

15. A system as set forth in claim 10, wherein the detection circuit comprises means for minimizing the disruption of the DC voltage of the POTS differential line pair by the detection circuit.

16. A system as set forth in claim 15, wherein the means for minimizing disruption includes a low pass filter.

17. A system as set forth in claim 16, wherein the detection circuit further comprises a protection circuit portion configured to minimize effects of anomalous voltage and current conditions on the differential line pair on the microcontroller.

18. A system as set forth in claim 10, wherein the detector circuit is configured to function regardless of polarity of the differential line pair.

19. A system as set forth in claim 14, wherein the programmed microcontroller comprises means to minimize the effects of noise on the differential line pair on detection of the DC state of the differential line pair.

20. A system as set forth in claim 10, wherein the pulse signals are square wave pulse signals.

21. A system as set forth in claim 20, wherein the pulse signals are initiated at time intervals of less than 16 milliseconds.

22. A system as set forth in claim 21, wherein the pulse signals are less than 20 microseconds in length from positive edge to negative edge.

23. A system as set forth in claim 14, wherein the microcontroller includes a data link capability to communicate with another processor.

24. A system as set forth in claim 23, wherein the microcontroller capability is minimized and timing and logic functions are moved to said another processor.

25. A system as set forth in claim 23, wherein the microprocessor capability is maximized and the detection circuit is connected to a user interface.

26. A system as set forth in claim 23, wherein the detection circuit is implemented on a PC card.

27. A system as set forth in claim 23, wherein the detection circuit is implemented in a separately powerable unit data connectable to a computer.

28. A system configured for a detection of at least one of a ring condition and off hook condition on a differential line pair in a telephone network, comprising:

a low pass filter comprising a first and second resistor on a first line of a differential line pair and a third and fourth resistor on a second line of the differential line pair, wherein a first capacitor is electrically coupled to the first line and second

line between the first and second resistor of the first line and the third and fourth resistor of the second line;

a bias circuit portion electrically coupled to an output of the low pass filter comprising a first Zener diode in series with and in opposite polarity from and a second Zener diode, each Zener diode having a break down voltage so that a change in voltage can be detected on either the first line and the second line of the differential line pair;

a DC isolation circuit portion electrically coupled to an output of the bias circuit comprising a second capacitor on the first line of the differential line pair and a third capacitor on the second line of the differential line pair;

a protection circuit portion connected to an output of the DC isolation circuit for protecting surges and spikes in a differential line; and

a microcontroller for detecting the state of the differential line pair having a digital output coupled to the second line for generating pulses and having an input electrically coupled to the first line of the differential line pair for detecting whether the pulses are present at a voltage level greater than a preset level.

29. A system configured for a detection of at least one of a ring condition and off hook condition on a differential line pair in a telephone network, comprising:

a low pass filter electrically coupled to a bias circuit;

the bias circuit wherein a first Zener diode is in series with and in opposite polarity from and a second Zener diode, each Zener diode having a break down voltage so that a change in voltage can be detected between on either a first line and a second line on a differential line pair;

a DC isolation circuit electrically coupled to the bias circuit and electrically coupled to a protection circuit for protecting surges and spikes in the differential line; and

a microcontroller having a digital output coupled to a line on the differential line pair for generating pulses and having an input electrically coupled to the other line of the differential line pair for detecting whether the pulses are present at a voltage level greater than a preset level.

30. A method for measuring a change in DC voltage on a differential line pair used in a telephone network connected to a microcontroller, comprising the steps of:

injecting a pulse signal from a microprocessor onto a first line of a differential line pair;

biasing the differential line pair with a bias circuit comprising a first Zener diode that is in series with and in opposite polarity to a second Zener diode, each Zener diode having a break down voltage so that a change in voltage can be detected on either the first line or a second line of the differential line pair;

isolating the microcontroller from a DC voltage on the differential line pair;

protecting the microcontroller from surges and spikes on the differential line pair;

detecting the microcontroller-generated pulse on the second line of the differential line pair with the microprocessor when the voltage difference between the first line of the differential line pair and the second line of the differential line pair is greater than a preset level.